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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,085	11/27/2001	Yoshiyuki Uchinono	11411/002001	9568
22511	7590	03/10/2004	EXAMINER	
ROSENTHAL & MAY L.L.P. 1221 MCKINNEY STREET HOUSTON, TX 77010			DINH, TUAN T	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/995,085

Applicant(s)

UCHINONO ET AL.

Examiner

Tuan T Dinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 and 5-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 5-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nellissen (U. S. Patent 5,937,493) in view of Roberts (U. S. Patent 5,584,120).

As to claim 1, Nellissen discloses a multilayer circuit board as shown in figures 1-9 comprising:

a substrate (9, column 6, line 27) having first and second surfaces (100, 200-figures 4-6, see attached paper has been explained in office action paper #12) extending from an end and the first surface at a required angle relative to the first surface;

a multilayer circuit (13, 15, 19) formed on the first surface of said substrate and composed of a plurality of circuit layers (see figures 6-9), each of which is provided with a conductive layer (13, column 6, lines 29-34) having a required circuit pattern and an insulation layer (15, column 6, lines 43-44) formed on said conductive layer;

a second conductive layer (19, column 6, line 52) formed on the second surface (200, see attached paper) of said substrate by which said conductive layer of one of

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said circuit layers is electrically to said conductive layer of another one of said circuit layers (13, 15, and 19).

The limitation "an insulation layer formed on said conductive layer by firm formation" has been consider. However, the presence of process limitation in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multiplayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface (200) of said substrate (9) includes a side surface (200') of a projection (5) on the first surface (100), **see attaching drawing papers in office action paper #12.**

Nellissen does not disclose the first surface is a top surface of said substrate, and the second surface further includes a side surface of said substrate, and the required angle between the first and second surfaces is an obtuse angle.

Roberts shows a multiplayer circuit board as shown in figures 1-10 comprising a substrate (1) having a first surface (16), which is a top surface of the substrate (1) and a second surface (15), which is a side surface of the substrate, the require angle between the first and second surfaces is an obtuse angle.

It would have been obvious to one having skill in the art at the time the invention was made to employ a first surface on top of a second surface including a side surface and having an obtuse angle in the multiplayer circuit board of Nellissen, as taught by

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Roberts, in order to provide a reliability and flexibility of a circuit design for the multilayer circuit board.

As to claim 6, Nellissen discloses a multilayer circuit board as shown in figures 1-15 wherein said second conductive layer (19) is a plurality of second conductive layers (23) to obtain plural layer-to-layer connections of said multilayer circuit, each of second conductive layers (23) is separated from an adjacent second conductive layer (19) in the thickness direction by a second insulation layer (21).

As to claim 5, Nellissen discloses a multilayer circuit board as shown in figures 1-15 comprising:

a substrate (9, column 6, line 27) having first and second surfaces (100, 200-figures 4-6, see attached paper in the office action paper #12) extending from an end and the first surface at a required angle relative to the first surface;

a multilayer circuit (13, 15, 19) formed on the first surface of said substrate and composed of a plurality of circuit layers (see figures 6-9), each of which is provided with a conductive layer (13, column 6, lines 29-34) having a required circuit pattern and an insulation layer (15, column 6, lines 43-44) formed on said conductive layer;

a second conductive layer (19, column 6, line 52) formed on the second surface (200) of said substrate by which said conductive layer of one of said circuit layers is electrically to said conductive layer of another one of said circuit layers (13, 15, and 19);

wherein said multilayer circuit has an aperture (7-figure 2, column 6, lines 24-25), through which a part of the first surface is exposed, and an electronic device (37, column 7, lines 45-50)) is mounted in a concave formed in the exposed first surface,

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and an electrical connection between said multilayer circuit and said electronic device is made by a third conductive layer (29, column 7, line 8) formed on an inner surface of said concave.

The limitation "an insulation layer formed on said conductive layer by firm formation" has been consider. However, the presence of process limitation in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multiplayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface (200) of said substrate (9) includes a side surface of a projection (5) on the first surface (100).

Nellissen does not disclose the first surface is a top surface of said substrate, and the second surface includes a side surface of said substrate, and the required angle between the first and second surfaces is an obtuse angle.

Roberts shows a multiplayer circuit board as shown in figures 1-10 comprising a substrate (1) having a first surface (16), which is a top surface of the substrate (1) and a second surface (15), which is a side surface of the substrate, the require angle between the first and second surfaces is an obtuse angle.

It would have been obvious to one having skill in the art at the time the invention was made to employ a first surface on top of a second surface including a side surface and having an obtuse angle in the multiplayer circuit board of Nellissen, as taught by

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Roberts, in order to provide a reliability and flexibility of a circuit design for the multilayer circuit board.

As to claim 7, Nellissen discloses a multilayer circuit board as shown in figures 1-15 comprising:

a substrate (9, column 6, line 27) having first and second surfaces (100, 200-figures 4-6) extending from an end and the first surface at a required angle relative to the first surface;

a multilayer circuit (13, 15, 19) formed on the first surface of said substrate and composed of a plurality of circuit layers (see figures 6-9), each of which is provided with a conductive layer (13, column 6, lines 29-34) having a required circuit pattern and an insulation layer (15, column 6, lines 43-44) formed on said conductive layer;

a second conductive layer (19, column 6, line 52) formed on the second surface (200) of said substrate by which a layer-layer connection of said multilayer circuit is made (13, 15, and 19);

wherein said substrate (9) has a third surface (300) extending at a different level from the first surface and a fourth surface (400) extending from the other end of the first surface to an end of the third surface (see figure 2 of the attaching drawing papers), and said multilayer circuit is formed on the first, third and fourth surfaces of said substrate, and said second conductive layer is formed on a side surface of a projection on the first surface to make the layer-to-layer connection of said multilayer circuit.

The limitation "an insulation layer formed on said conductive layer by firm formation" has been consider. However, the presence of process limitation in product

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claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multiplayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface (200) of said substrate (9) includes a side surface of a projection (5) on the first surface (100).

Nellisen does not disclose the first surface is a top surface of said substrate, and the second surface includes a side surface of said substrate, and the required angle between the first and second surfaces is an obtuse angle.

Roberts shows a multiplayer circuit board as shown in figures 1-10 comprising a substrate (1) having a first surface (16), which is a top surface of the substrate (1) and a second surface (15), which is a side surface of the substrate, the require angle between the first and second surfaces is an obtuse angle.

It would have been obvious to one having skill in the art at the time the invention was made to employ a first surface on top of a second surface including a side surface and having an obtuse angle in the multiplayer circuit board of Nellissen, as taught by Roberts, in order to provide a reliability and flexibility of a circuit design for the multiplayer circuit board.

As to claim 8, Nellissen discloses a multilayer circuit board as shown in figures 1-9 comprising:



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a substrate (9) having a first surface (100) and a projection (5) formed on the first surface;

a pair of multilayer circuits (13, 15, 19, 21, 23, and 25-figures 5-9) formed on the first surface (100) at both sides of said projection (5), each of said multilayer circuits (13,15; 19,21, 23) composed of a plurality of circuit layers, each of which is provided with a conductive-metal layer (13, 19, or 23) having a required circuit pattern and an insulation layer (15; 21, or 25) formed on said conductive-metal layer; and

a second conductive-metal layer (19-figure 6) successively formed on side and top surfaces of said projection (5),

wherein said conductive-metal layer of one of said circuit layers is electrically connected to said conductive layer of another one of said circuit layers by said second conductive-metal layer on the side surface of said projection (13, 15, and 19), and one of the pair of multilayer circuits (13, 15) is electrically connected to the other one (21, 23) by said second conductive-metal layer (19) on the side and top surfaces of said projection (see figure 8).

The limitation "an insulation layer formed on said conductive layer by firm formation" has been consider. However, the presence of process limitation in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multiplayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface

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(200) of said substrate (9) includes a side surface of a projection (5) on the first surface (100).

Nellissen does not disclose the angle between the side surface of the projection and the first surface is an obtuse angle.

Roberts shows a multiplayer circuit board as shown in figures 1 and 5 comprising a substrate (1) having a first surface (16) and a side surface of a projection (see figure 5), and the require angle between the first surface is an obtuse angle.

It would have been obvious to one having skill in the art at the time the invention was made to employ the angle between a first surface and a side surface of a projection having an obtuse angle in the multiplayer circuit board of Nellissen, as taught by Roberts, in order to provide a high density contact clusters and an ability for manufacture low cost.

As to claim 9, Nellissen discloses said multilayer circuit has an aperture (7-figure 2, column 6, lines 24-25), through which a part of the first surface is exposed, and an electronic device (37, column 7, lines 45-50)) is mounted in a concave formed in the exposed first surface, and an electrical connection between said multilayer circuit and said electronic device is made by a third conductive layer (29, column 7, line 8) formed on an inner surface of said concave.

As to claim 10, Nellissen discloses a multilayer circuit board as shown in figures 1-15 wherein said second conductive layer (19) is a plurality of second conductive layers (23) to obtain plural layer-to-layer connections of said multilayer circuit, each of

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second conductive layers (23) is separated from an adjacent second conductive layer (19) in the thickness direction by a second insulation layer (21).

As to claim 11, Nellissen discloses in figure 13 further comprising a third conductive-metal layer (33), which is formed on a side surface of said substrate extending adjacent to the first surface.

### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1, and 5-11 have been considered but are moot in view of the new ground(s) of rejection.

#### **Applicant argues:**

(a) Nellissen does not teach "a second conductive layer...on the first surface"

(b) Nellissen does not teach "layer to layer connections between conductive layers in the multiplayer circuits"

#### **Examiner disagrees.**

Response to argument (a), Nellissen clearly shows in figures 4-9 that a conductive layer (19) formed on a second surface (200) of a substrate (9) in which said conductive layer of one of said circuit layers (13 is electrically connected to said conductive layer of another one of said circuit layers (Nellisen discloses a conductive 13 deposit on a first surface of substrate 9 and a projection 5 in a direction of an arrow A having an angle approximately 50 degrees, and hide behind the projection 5 which is continuous connection through the first and the second surfaces, and also see figures

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2-6, Nellissen discloses the second surface (200) including a side surface (200') of a projection (5) on a first surface (100).

Response to argument (b), Nellissen clearly shows the circuit layers (13, 15, 19, 21, 23, or 25) deposit on a surface of the substrate (9). The deposition layers (13, 15, 19, 21, 23, or 25) on the substrate, which can be seen from a delta angle as shown in figures 4-9 that are layer-layer connections. For example, figure 4 shows the view from right to left at a delta angle, the conductive layer 13 is continuous deposit on the surface of the substrate 9, and in figure 6 also shows the view from left to right at the delta angle, the conductive layer 19 is continuous deposit on the surface of the substrate.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh  
February 17, 2004.



**EVAN PERT**  
**PRIMARY EXAMINER**